

# National Testing Agency

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## A Practical Refresher in Computer Engineering

**Group Number :** 1  
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## A Practical Refresher in Computer Engineering

**Section Id :** 28860724  
**Section Number :** 1  
**Section type :** Online  
**Mandatory or Optional:** Mandatory  
**Number of Questions:** 70  
**Number of Questions to be attempted:** 70  
**Section Marks:** 140

**Sub-Section Number:** 1  
**Sub-Section Id:** 28860724  
**Question Shuffling Allowed :** Yes

**Question Number : 1 Question Id : 2886071886 Question Type : MCQ Option Shuffling : No**  
**Correct Marks : 2 Wrong Marks : 1**

The von Neumann architecture of a computer talks about: (choose the BEST option).

- higher level algorithms
- the stored program concept
- automata in hardware
- functional programming

Options :

2886077534. 1

2886077535. 2

2886077536. 3

2886077537. 4

Question Number : 2 Question Id : 2886071887 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is NOT an abstract component of a von Neumann computer?

- a. Control Path
- b. Data Path
- c. Management Path
- d. Memory

Options :

2886077538. 1

2886077539. 2

2886077540. 3

2886077541. 4

Question Number : 3 Question Id : 2886071888 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In MIPS32, the '32' indicates:

- a. The number of instructions possible
- b. The width in bits of the memory address
- c. The number of R-type instructions
- d. The number of pipeline stages

Options :

2886077542. 1

2886077543. 2

2886077544. 3

2886077545. 4

Question Number : 4 Question Id : 2886071889 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Given that MIPS32 uses 2's complement notation for the immediate operand, which ONE of the following is NOT a valid MIPS32 instruction?

- a. lw
- b. sw
- c. sub
- d. subi

Options :

2886077546. 1

2886077547. 2

2886077548. 3

2886077549. 4

Question Number : 5 Question Id : 2886071890 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following MIPS instructions would you use IDEALLY to multiply the value of a register by 4 ?

- a. mul
- b. muli
- c. sll
- d. srl

Options :

2886077550. 1

2886077551. 2

2886077552. 3

2886077553. 4

Question Number : 6 Question Id : 2886071891 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In the MIPS32 instruction set, branch based on if-less-than comparison \_\_\_\_\_

- a. is not supported at all
- b. is supported in a single instruction
- c. is supported as a pair of instructions
- d. is possible only if one of the values is zero

Options :

2886077554. 1

2886077555. 2

2886077556. 3

2886077557. 4

Question Number : 7 Question Id : 2886071892 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In MIPS, callee-saved registers are also called \_\_\_\_\_.

- a. preserved
- b. unpreserved
- c. intermediate
- d. shadow

Options :

2886077558. 1

2886077559. 2

2886077560. 3

2886077561. 4

Question Number : 8 Question Id : 2886071893 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In MIPS, callee-saved registers are saved onto \_\_\_\_\_.

- a. swap memory
- b. the process stack
- c. dynamic heap memory
- d. static global memory

Options :

2886077562. 1

2886077563. 2

2886077564. 3

2886077565. 4

Question Number : 9 Question Id : 2886071894 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following integer notations has a unique representation for the number 0 ?

- a. sign-magnitude
- b. 1's complement
- c. 2's complement
- d. None of the other options

Options :

2886077566. 1

2886077567. 2

2886077568. 3

2886077569. 4

Question Number : 10 Question Id : 2886071895 Question Type : MCQ Option Shuffling : No  
Correct Marks : 2 Wrong Marks : 1

In a MIPS program's memory, the global data is placed at the bottommost portion (lowest address starting from 0) of memory: \_\_\_\_\_. (choose the BEST option below).

- a. only when the program is statically linked
- b. when the program has no dynamically allocated data
- c. never
- d. when the program has no function calls

Options :

2886077570. 1

2886077571. 2

2886077572. 3

2886077573. 4

Question Number : 11 Question Id : 2886071896 Question Type : MCQ Option Shuffling : No  
Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is true about the \$at (assembler temporary) register in MIPS32 ?

- a. It is preserved, and it is temporarily stored in the heap
- b. It is preserved, and it is temporarily stored in the stack frame
- c. It is preserved, but it is not stored in the stack
- d. It is caller-saved

Options :

2886077574. 1



2886077575. 2

2886077576. 3

2886077577. 4

Question Number : 12 Question Id : 2886071897 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is true about the \$ra (return address) register in MIPS32 ?

- a. It is preserved, and it is temporarily stored in the heap
- b. It is preserved, and it is temporarily stored in the stack frame
- c. It is unpreserved
- d. It always has the value of 0xFFFFFFFF

Options :

2886077578. 1

2886077579. 2

2886077580. 3

2886077581. 4

Question Number : 13 Question Id : 2886071898 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In the context of computer performance quantification, SPEC is \_\_\_\_\_..

- a. a particular computer architecture with a rich instruction set
- b. a specification language for formal performance bounds
- c. a compiler with many optimization techniques
- d. a consortium of computer industries

Options :

2886077582. 1

2886077583. 2

2886077584. 3

2886077585. 4

Question Number : 14 Question Id : 2886071899 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which of the components of the computer performance equation does the choice of HLL (Higher Level Language) affect ? Choose the BEST option below.

- a. Only the number of instructions
- b. Only the cycle time
- c. Both the number of instructions and the cycle time
- d. Neither the number of instructions nor the cycle time

Options :

2886077586. 1

2886077587. 2

2886077588. 3

2886077589. 4

Question Number : 15 Question Id : 2886071900 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which of the components of the computer performance equation does the instruction set architecture affect ? Choose the BEST option below.

- a. Only the number of instructions
- b. Only the CPI
- c. Both the number of instructions and the CPI
- d. Neither the number of instructions nor the CPI

Options :

2886077590. 1

2886077591. 2

2886077592. 3

2886077593. 4

Question Number : 16 Question Id : 2886071901 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is a valid return statement from an exception handler in a MIPS32 machine?

- a. jalr \$ra
- b. jr \$ra
- c. jr \$k0
- d. jalr \$at

Options :

2886077594. 1

2886077595. 2

2886077596. 3

2886077597. 4

Question Number : 17 Question Id : 2886071902 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following limits the achievable performance improvement in a computer?

- a. Huddle space constraint
- b. Magnolias effect
- c. Amdahl's law
- d. Little's theorem

Options :

2886077598. 1

2886077599. 2

2886077600. 3

2886077601. 4

Question Number : 18 Question Id : 2886071903 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

A program's CPI (Cycles Per Instruction) will most likely NOT be affected by the use of:  
(choose the BEST option)

- a. integer versus floating point arithmetic
- b. signed versus unsigned integers for small positive integer variables
- c. optimization techniques employed by the compiler
- d. memory versus compute intensive algorithm

Options :

2886077602. 1

2886077603. 2

2886077604. 3

2886077605. 4

Question Number : 19 Question Id : 2886071904 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1



In the MIPS32 5-stage pipeline, a sw followed by a lw causes a data hazard stall on a memory location (not a register) \_\_\_\_\_ .

- a. always
- b. never
- c. when the lw loads the base register of sw
- d. when the sw stores the base register of lw

Options :

2886077606. 1

2886077607. 2

2886077608. 3

2886077609. 4

Question Number : 20 Question Id : 2886071905 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In the MIPS32 5-stage pipeline, a lw followed by another lw causes a data hazard stall \_\_\_\_\_ .

- a. always
- b. never
- c. when the first lw loads the base register of the second lw
- d. when the second lw loads the base register of the first lw

Options :

2886077610. 1

2886077611. 2

2886077612. 3

2886077613. 4

Question Number : 21 Question Id : 2886071906 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In the MIPS32 5-stage pipeline, a sw followed by another sw causes a data hazard stall \_\_\_\_\_ .

- a. always
- b. never
- c. when the first sw stores the base register of the second sw
- d. when the second sw stores the base register of the first sw

Options :

2886077614. 1

2886077615. 2

2886077616. 3

2886077617. 4

Question Number : 22 Question Id : 2886071907 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is true about structural hazards in a pipelined processor?

- a. they will result in performance degradation
- b. they will result in OS deadlocks
- c. they can be handled using data forwarding
- d. they can be handled using branch prediction

Options :

2886077618. 1

2886077619. 2

2886077620. 3

2886077621. 4

Question Number : 23 Question Id : 2886071908 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In the MIPS32 5-stage pipeline implementation, the register file is written in the first half and read in the second half of a cycle. Why? (choose the BEST option below).

- a. This avoids expensive structural hazards in the register file for each instruction
- b. This reduces instances of control hazard stalls
- c. This reduces chances of pipeline exceptions
- d. This leads to lesser cache misses

Options :

2886077622. 1

2886077623. 2

2886077624. 3

2886077625. 4

Question Number : 24 Question Id : 2886071909 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is an implication of control hazards in the MIPS32 5-stage pipeline?

- a. branch instructions take 6 cycles to complete instead of 3
- b. there are extra stalls in the pipeline after each branch instruction
- c. structural hazards in branches face twice as many stalls compared to other instructions
- d. data forwarding becomes ineffective

Options :

2886077626. 1

2886077627. 2

2886077628. 3

2886077629. 4

Question Number : 25 Question Id : 2886071910 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

The technique of loop unrolling can lead to lesser pipeline stalls. Which entity is responsible for such unrolling?

- a. Operating System
- b. Dynamic Linker
- c. Compiler
- d. Terminal Shell

Options :

2886077630. 1

2886077631. 2

2886077632. 3

2886077633. 4

Question Number : 26 Question Id : 2886071911 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is a compiler's role, in reducing branch penalty in the pipeline?

- a. replacing conditional branches with unconditional branches
- b. replacing unconditional branches with conditional branches
- c. scheduling useful instructions in the branch delay slot
- d. making branch instructions always use the fp (frame pointer) register

Options :

2886077634. 1



2886077635. 2

2886077636. 3

2886077637. 4

Question Number : 27 Question Id : 2886071912 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In the MIPS32 5-stage pipeline, what is the ideal CPI (Cycles Per Instruction), in the absence of hazards and stalls?

- a. 1/5
- b. 1
- c. 3
- d. 5

Options :

2886077638. 1

2886077639. 2

2886077640. 3

2886077641. 4

Question Number : 28 Question Id : 2886071913 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following techniques is for the purpose of reducing control hazards, and requires the role of the operating system?

- a. branch prediction
- b. early branch completion
- c. branch target buffer
- d. none of the other options

Options :

2886077642. 1

2886077643. 2

2886077644. 3

2886077645. 4

Question Number : 29 Question Id : 2886071914 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1



In the MIPS32 5-stage pipeline, an add instruction is followed by a jump instruction. Unconditional branches take 2 cycles to complete. There is NO mechanism other than stalls to deal with control hazards. How many cycles of stall are required and when?

- a. 1 cycle, between the add and jump
- b. 1 cycle, after the jump
- c. 2 cycles, between the add and jump
- d. 2 cycles, after the jump

Options :

2886077646. 1

2886077647. 2

2886077648. 3

2886077649. 4

Question Number : 30 Question Id : 2886071915 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is true about 2-stage branch completion in the MIPS32 5-stage pipeline?

- a. this is possible only for unconditional branches
- b. this potentially introduces additional data hazards
- c. this requires the compiler to arrange branch instructions to be within 4 instructions of one another
- d. this requires the branch offset to be less than 256 in absolute value

Options :

2886077650. 1

2886077651. 2

2886077652. 3

2886077653. 4

Question Number : 31 Question Id : 2886071916 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In MIPS32, a branch delay slot can ALWAYS be safely filled with an instruction from \_\_\_\_\_.

- a. before the branch
- b. the branch fall through
- c. the branch target
- d. none of the other options

Options :

2886077654. 1

2886077655. 2

2886077656. 3

2886077657. 4

Question Number : 32 Question Id : 2886071917 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In MIPS32, a branch delay slot can NEVER be filled with a \_\_\_\_\_ instruction.

- a. nop
- b. load word
- c. store word
- d. jump

Options :

2886077658. 1

2886077659. 2

2886077660. 3

2886077661. 4

Question Number : 33 Question Id : 2886071918 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is true about 2-stage branch completion in the MIPS32 5-stage pipeline, compared to 3-stage branch completion?

- a. extra delay slots are required
- b. extra data forwarding paths are required
- c. extra instruction formats are required
- d. extra CPU cores are required

Options :

2886077662. 1

2886077663. 2

2886077664. 3

2886077665. 4

Question Number : 34 Question Id : 2886071919 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In the MIPS32 5-stage pipeline, which ONE of the following is true about a STALL introduced due to a data hazard, specifically, lw followed by a dependent add ?

- a. The STALL introduces a nop between the lw and the add in the pipeline
- b. The STALL introduces a nop before the lw in the pipeline
- c. The STALL introduces a nop after the add in the pipeline
- d. The STALL introduces two nops: one before and one after the add in the pipeline

Options :

2886077666. 1

2886077667. 2

2886077668. 3

2886077669. 4

Question Number : 35 Question Id : 2886071920 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In a pipelined processor, code executed by a simpler processor within the main processor (toward implementing pipeline control) is called \_\_\_\_\_. Choose the BEST option below.

- a. lambda code
- b. micro-code
- c. machine code
- d. pseudo-code

Options :

2886077670. 1

2886077671. 2

2886077672. 3

2886077673. 4

Question Number : 36 Question Id : 2886071921 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following kinds of RAM is used in cache memory in typical computers? Choose the BEST option.

- a. Static RAM
- b. Dynamic RAM
- c. Distributed RAM
- d. Synchronized RAM

Options :

2886077674. 1



2886077675. 2

2886077676. 3

2886077677. 4

Question Number : 37 Question Id : 2886071922 Question Type : MCQ Option Shuffling : No  
Correct Marks : 2 Wrong Marks : 1

In the MIPS32 5-stage pipeline, at the END of which stage can an invalid opcode exception be detected?

- a. IF
- b. ID
- c. EX
- d. MEM

Options :

2886077678. 1

2886077679. 2

2886077680. 3

2886077681. 4

Question Number : 38 Question Id : 2886071923 Question Type : MCQ Option Shuffling : No  
Correct Marks : 2 Wrong Marks : 1

In a computer's cache system, a block refers to: (choose the BEST option below)

- a. the unit of data in L1 cache
- b. the unit of data in L2 cache
- c. the unit of data transfer into cache during a cache miss
- d. the unit of data transfer from cache during a cache hit

Options :

2886077682. 1

2886077683. 2

2886077684. 3

2886077685. 4

Question Number : 39 Question Id : 2886071924 Question Type : MCQ Option Shuffling : No  
Correct Marks : 2 Wrong Marks : 1



In a cache system, which ONE of the following mechanisms takes advantage of spatial locality? Choose the BEST option below.

- a. Multiple words per block
- b. Large tag size
- c. Parallel tag comparators
- d. Unified I+D cache

Options :

2886077686. 1

2886077687. 2

2886077688. 3

2886077689. 4

Question Number : 40 Question Id : 2886071925 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

A system has 1MB of main memory and 2KB of cache. It uses a direct mapped scheme and blocks of size 1 word (32 bits). What is the size (number of bits) of the tag field in the memory address? Take  $1M = 2^{20}$  and  $1K = 2^{10}$ .

- a. 8 bits
- b. 9 bits
- c. 2K bits
- d. 1M bits

Options :

2886077690. 1

2886077691. 2

2886077692. 3

2886077693. 4

Question Number : 41 Question Id : 2886071926 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

If an L1 cache's associativity is changed from 8-way to 16-way, keeping its overall size the same, how is the size of the tag field in a block affected?

- a. increases by 8 bits
- b. decreases by 8 bits
- c. increases by 1 bit
- d. decreases by 1 bit

Options :

2886077694. 1

2886077695. 2

2886077696. 3

2886077697. 4

Question Number : 42 Question Id : 2886071927 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is TRUE about L1 vs L2 caches? Choose the BEST option below.

- a. L1 is typically smaller in size, to minimize hit time
- b. L2 is typically direct mapped, to minimize miss rate
- c. L1 is typically smaller in size, to minimize miss rate
- d. L2 typically has higher associativity, to minimize hit time

Options :

2886077698. 1

2886077699. 2

2886077700. 3

2886077701. 4

Question Number : 43 Question Id : 2886071928 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

A cache is k-way associative. Here, k refers to \_\_\_\_ (choose the BEST option below).

- a. the cache block size
- b. the number of TLB entries
- c. the number of sets in the cache
- d. the number of blocks in a set

Options :

2886077702. 1

2886077703. 2

2886077704. 3

2886077705. 4

Question Number : 44 Question Id : 2886071929 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is TRUE about unified I+D cache versus separate I/D caches ? Choose the BEST option below.

- a. A unified cache scheme rules out the use of branch delay slots
- b. A separate I/D cache scheme rules out the use of branch delay slots
- c. A unified cache scheme leads to less control hazards
- d. A separate I/D cache scheme leads to less structural hazards

Options :

2886077706. 1

2886077707. 2

2886077708. 3

2886077709. 4

Question Number : 45 Question Id : 2886071930 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In the context of L1 cache in a computer, when is hit ratio + miss ratio = 1 ?

- a. Always
- b. Never
- c. Only when program size is below an L1 block
- d. Only when program size is below an L2 block

Options :

2886077710. 1

2886077711. 2

2886077712. 3

2886077713. 4

Question Number : 46 Question Id : 2886071931 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is a DISADVANTAGE of larger block size? Choose the BEST option below.

- a. higher hit time
- b. higher miss penalty
- c. higher compulsory misses
- d. higher overhead in terms of tag bits

Options :

2886077714. 1

2886077715. 2

2886077716. 3

2886077717. 4

Question Number : 47 Question Id : 2886071932 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1



Which ONE of the following techniques can reduce miss penalty from L1 cache ?

Choose the BEST option below.

- a. decreasing cache block size
- b. increasing cache block size
- c. increasing swap space
- d. disabling interrupts

Options :

2886077718. 1

2886077719. 2

2886077720. 3

2886077721. 4

Question Number : 48 Question Id : 2886071933 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In a virtual memory based system, the granularity at which two processes can share memory is \_\_\_\_ (choose the BEST option below).

- a. a memory page
- b. a disk cylinder
- c. a TLB table
- d. a file on disk

Options :

2886077722. 1

2886077723. 2

2886077724. 3

2886077725. 4

Question Number : 49 Question Id : 2886071934 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In a virtual memory based system, two processes can share memory \_\_\_\_\_ (choose the BEST option below).

- a. only in the data memory
- b. only in the instruction memory
- c. only in exception memory
- d. none of the other options

Options :

2886077726. 1

2886077727. 2



2886077728. 3

2886077729. 4

Question Number : 50 Question Id : 2886071935 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is an ADVANTAGE of the interleaved memory scheme compared to the original wide-memory scheme? Choose the BEST option below.

- a. lower miss penalty
- b. lower hardware cost
- c. lower hit time
- d. lower miss rate

Options :

2886077730. 1

2886077731. 2

2886077732. 3

2886077733. 4

Question Number : 51 Question Id : 2886071936 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

When someone says they have a 32-bit machine or a 64-bit machine, what does this refer to?

- a. The virtual memory address length
- b. The physical memory address length
- c. The width of the cache-main-memory bus
- d. The width of the main-mem-disk bus

Options :

2886077734. 1

2886077735. 2

2886077736. 3

2886077737. 4

Question Number : 52 Question Id : 2886071937 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

When Virtual Memory is used for easing program relocation, \_\_\_\_\_ (choose the BEST option below).

- a. The OS automatically rewrites the necessary program instructions
- b. The hardware automatically changes the meaning of various opcodes
- c. The process's page table entries are changed to reflect the relocation
- d. The location of the process's page table is changed to reflect the relocation

Options :

2886077738. 1

2886077739. 2

2886077740. 3

2886077741. 4

Question Number : 53 Question Id : 2886071938 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following metrics is the MOST important to minimize for a TLB ?

- a. miss rate
- b. miss penalty
- c. lock overhead
- d. sync delay

Options :

2886077742. 1

2886077743. 2

2886077744. 3

2886077745. 4

Question Number : 54 Question Id : 2886071939 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

When Virtual Memory is used to provide isolation across processes, \_\_\_\_\_ (choose the BEST option below).

- a. each process's page table entries are made read-only for other processes
- b. each process's memory locations are made read-only for other processes
- c. each process's page table has mappings to only pages it is allowed to access
- d. when a process is executing, the pages of other processes are moved to swap space

Options :

2886077746. 1

2886077747. 2

2886077748. 3

2886077749. 4

Question Number : 55 Question Id : 2886071940 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following instructions changes the processor execution mode from application mode to kernel mode?

- a. jalr (jump and link register)
- b. condj (conditional jump)
- c. syscall (system call)
- d. lw (load word)

Options :

2886077750. 1

2886077751. 2

2886077752. 3

2886077753. 4

Question Number : 56 Question Id : 2886071941 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which of the following is/are used as keys in the hashtable mapping, in the inverted page table scheme ? Choose the BEST option below.

- a. Only Process ID
- b. Only Processor core number
- c. Process ID and Processor core number
- d. Process ID and Virtual page number

Options :

2886077754. 1

2886077755. 2

2886077756. 3

2886077757. 4

Question Number : 57 Question Id : 2886071942 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1



In a pipelined processor, TLB access is typically implemented \_\_\_\_\_ in the common case. (choose the BEST option below).

- a. by an OS exception handler
- b. in a co-processor
- c. as a pipeline stage, or part of a pipeline stage
- d. in the I/O bus controller

Options :

2886077758. 1

2886077759. 2

2886077760. 3

2886077761. 4

Question Number : 58 Question Id : 2886071943 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

The sed tool is used for \_\_\_\_\_ (choose the BEST option below).

- a. line-by-line processing of text files
- b. filtering records in a database
- c. processing SQL files
- d. processing a.out files

Options :

2886077762. 1

2886077763. 2

2886077764. 3

2886077765. 4

Question Number : 59 Question Id : 2886071944 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

In a bash script, how are comments represented?

- a. Using a '#' anywhere in a line
- b. Using a '\$' anywhere in a line
- c. Between /% and %/
- d. Between \$# and # \$

Options :

2886077766. 1

2886077767. 2

2886077768. 3



2886077769. 4

Question Number : 60 Question Id : 2886071945 Question Type : MCQ Option Shuffling : No  
Correct Marks : 2 Wrong Marks : 1

In the context of programming, a "loop invariant" is: (choose the BEST option below)

- a. A variable which is declared inside the loop
- b. A variable which is declared outside the loop
- c. A #define pre-processor macro defined in a static library
- d. A condition which must hold at the beginning/end of each loop iteration

Options :

2886077770. 1

2886077771. 2

2886077772. 3

2886077773. 4

Question Number : 61 Question Id : 2886071946 Question Type : MCQ Option Shuffling : No  
Correct Marks : 2 Wrong Marks : 1

In a bash shell, when a program is running in the foreground, Ctrl-C is pressed. Which ONE of the following is most likely to happen?

- a. The program starts executing in another processor core
- b. The program priority is lowered
- c. The program is terminated
- d. The program is suspended

Options :

2886077774. 1

2886077775. 2

2886077776. 3

2886077777. 4

Question Number : 62 Question Id : 2886071947 Question Type : MCQ Option Shuffling : No  
Correct Marks : 2 Wrong Marks : 1

In a bash script, the use of '|' (pipe) does the following: (choose the BEST option below).

- a. runs a program as multiple threads
- b. makes a program run in the background
- c. uses multiple processor cores to run a program
- d. takes STDIN of a process from STDOUT of another

Options :

2886077778. 1

2886077779. 2

2886077780. 3

2886077781. 4

Question Number : 63 Question Id : 2886071948 Question Type : MCQ Option Shuffling : No  
Correct Marks : 2 Wrong Marks : 1

In python3,  $x=2$  and  $y=[3,2]$ . To get the list  $[3,2,3,2]$ , we can use the expression:

- a. `lambda(x,y)`
- b. `x*y`
- c. `map(x,y)`
- d. None of the other options

Options :

2886077782. 1

2886077783. 2

2886077784. 3

2886077785. 4

Question Number : 64 Question Id : 2886071949 Question Type : MCQ Option Shuffling : No  
Correct Marks : 2 Wrong Marks : 1

In python, a lambda expression is used to: (choose the BEST option below)

- a. create a function as a first class object
- b. create a sublist of a given list
- c. apply a convolution to elements of a list
- d. import objects from other libraries

Options :

2886077786. 1

2886077787. 2

2886077788. 3

2886077789. 4

Question Number : 65 Question Id : 2886071950 Question Type : MCQ Option Shuffling : No  
Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is NOT a git command?

- a. add
- b. clone
- c. push
- d. mine

Options :

2886077790. 1

2886077791. 2

2886077792. 3

2886077793. 4

Question Number : 66 Question Id : 2886071951 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is a tool used primarily for software version management?  
(choose the BEST option below).

- a. git
- b. eclipse
- c. emacs
- d. ps

Options :

2886077794. 1

2886077795. 2

2886077796. 3

2886077797. 4

Question Number : 67 Question Id : 2886071952 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

The lex tool allows the specification of additional code in which language? (Choose the BEST option below).

- a. C
- b. Python
- c. Java
- d. Javascript

Options :

2886077798. 1

2886077799. 2



2886077800. 3

2886077801. 4

Question Number : 68 Question Id : 2886071953 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

The yacc tool can be used to parse a \_\_\_\_\_

- a. context-free grammar
- b. Java class file
- c. Linux exe file
- d. JPG file in a web browser's cache

Options :

2886077802. 1

2886077803. 2

2886077804. 3

2886077805. 4

Question Number : 69 Question Id : 2886071954 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is true about object oriented programming in Java ?

- a. Only classes can be inherited/extended, not interfaces or exceptions
- b. Only classes and interfaces can be inherited/extended, not exceptions
- c. Only classes and exceptions can be inherited/extended, not interfaces
- d. Classes, exceptions, or interfaces can be inherited/extended

Options :

2886077806. 1

2886077807. 2

2886077808. 3

2886077809. 4

Question Number : 70 Question Id : 2886071955 Question Type : MCQ Option Shuffling : No

Correct Marks : 2 Wrong Marks : 1

Which ONE of the following is a difference between Object Oriented Programming in C++ versus Java. (choose the BEST option below).

- a. the feature of inheritance
- b. the notion of interfaces
- c. the notion of static variables
- d. the notion of constructor



Options :

2886077810. 1

2886077811. 2

2886077812. 3

2886077813. 4