

National Testing Agency

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A Practical Refresher In Computer Engineering

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A Practical Refresher In Computer Engineering-1

Section Id :	603489165
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Sub-Section Number :	1
Sub-Section Id :	603489292
Question Shuffling Allowed :	Yes

Question Number : 1 Question Id : 6034898040 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following is TRUE about unified I+D cache versus separate I/D caches ?
Choose the BEST option below.

1. A unified cache scheme rules out the use of branch delay slots
2. A separate I/D cache scheme rules out the use of branch delay slots
3. A unified cache scheme leads to less control hazards
4. A separate I/D cache scheme leads to less structural hazards

Options :

60348930135. 1

60348930136. 2

60348930137. 3

60348930138. 4

Question Number : 2 Question Id : 6034898041 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following is NOT a branch prediction scheme in a pipelined processor?

1. 1-bit predictor
2. 2-bit predictor
3. correlating predictor
4. multi-threaded predictor

Options :

60348930139. 1

60348930140. 2

60348930141. 3

60348930142. 4

Question Number : 3 Question Id : 6034898042 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

To reduce branch penalty, which ONE of the following techniques can be implemented in the MIPS-32 5-stage pipeline?

1. 1-stage instead of 3-stage branch completion
2. 2-stage instead of 3-stage branch completion
3. independent register file for branch instructions
4. separate instruction memory for branch instructions

Options :

60348930143. 1

60348930144. 2

60348930145. 3

60348930146. 4

Question Number : 4 Question Id : 6034898043 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In MIPS32, a branch delay slot can be safely filled with a jump instruction ____.

1. always
2. never
3. in programs using only integer registers
4. in programs using only temporary registers

Options :

60348930147. 1

60348930148. 2

60348930149. 3

60348930150. 4

Question Number : 5 Question Id : 6034898044 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In MIPS32, a branch delay slot can ALWAYS be safely filled with an instruction from ____.

1. before the branch
2. the branch fall through
3. the branch target
4. none of the above

Options :

60348930151. 1

60348930152. 2

60348930153. 3

60348930154. 4

Question Number : 6 Question Id : 6034898045 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In the MIPS32 5-stage pipeline, an add instruction is followed by a beq instruction. Conditional branches take 3 cycles to complete. There is NO mechanism other than stalls to deal with control hazards. How many cycles of stall are required and when?

1. 1 cycle, between the add and beq
2. 1 cycle, after the beq
3. 2 cycles, between the add and beq
4. 2 cycles, after the beq

Options :

60348930155. 1

60348930156. 2

60348930157. 3

60348930158. 4

Question Number : 7 Question Id : 6034898046 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In the MIPS32 5-stage pipeline implementation, the register file is written in the first half and read in the second half of a cycle. Why?

1. This leads to lesser cache misses
2. This avoids expensive structural hazards in the register file for each instruction
3. This reduces instances of control hazard stalls
4. This reduces chances of pipeline exceptions

Options :

60348930159. 1

60348930160. 2

60348930161. 3

60348930162. 4

Question Number : 8 Question Id : 6034898047 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following is an implication of control hazards in the MIPS32 5-stage pipeline?

1. Branch instructions take 6 cycles to complete instead of 3
2. Structural hazards in branches face twice as many stalls compared to other instructions
3. Data forwarding becomes ineffective
4. There are extra stalls in the pipeline after each branch instruction

Options :

60348930163. 1

60348930164. 2

60348930165. 3

60348930166. 4

Question Number : 9 Question Id : 6034898048 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following is true about structural hazards in a pipelined processor?

1. They can be handled in a pipelined implementation by data forwarding
2. They will not result in any performance degradation
3. They essentially mean that a pipelined implementation cannot be used
4. They can be handled in a pipelined implementation by introducing stalls

Options :

60348930167. 1

60348930168. 2

60348930169. 3

60348930170. 4

Question Number : 10 Question Id : 6034898049 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In the MIPS32 5-stage pipeline, a lw followed by another lw causes a data hazard stall on a memory location (not a register) ____ .

1. when the first lw loads the base register of the second lw
2. when the second lw loads the base register of the first lw
3. always
4. never

Options :

60348930171. 1

60348930172. 2

60348930173. 3

60348930174. 4

Question Number : 11 Question Id : 6034898050 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In the MIPS32 5-stage pipeline, a sw followed by a lw causes a data hazard stall ____ .

1. always
2. when the lw loads the base register of sw
3. when the sw stores the base register of lw
4. never

Options :

60348930175. 1

60348930176. 2

60348930177. 3

60348930178. 4

Question Number : 12 Question Id : 6034898051 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In the MIPS32 5-stage pipeline, a lw followed by a sw causes a data hazard stall ____ .

1. always
2. never
3. when the lw loads the base register of sw
4. when the sw stores the base register of lw

Options :

60348930179. 1

60348930180. 2

60348930181. 3

60348930182. 4

Question Number : 13 Question Id : 6034898052 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which hardware architecture talks about the stored program concept?

1. Amdahl's
2. Turing
3. Von Neumann
4. Donald Knuth

Options :

60348930183. 1

60348930184. 2

60348930185. 3

60348930186. 4

Question Number : 14 Question Id : 6034898053 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following is NOT an abstract component of a von Neumann computer?

1. Control Path
2. Data Path
3. Cache controller
4. Memory

Options :

60348930187. 1

60348930188. 2

60348930189. 3

60348930190. 4

Question Number : 15 Question Id : 6034898054 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In MIPS32, the '32' indicates:

1. The types of instructions possible
2. The width in bits of the memory address
3. The number of floating point instructions
4. The number of pipeline stages

Options :

60348930191. 1

60348930192. 2

60348930193. 3

60348930194. 4

Question Number : 16 Question Id : 6034898055 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Given that MIPS32 uses 2's complement notation for the immediate operand, which ONE of the following is a special MIPS32 instruction for unsigned integers?

1. LWU (Load Word Unsigned)
2. SWU (Store Word Unsigned)
3. subi (subtract integer)
4. addiu (add immediate unsigned)

Options :

60348930195. 1

60348930196. 2

60348930197. 3

60348930198. 4

Question Number : 17 Question Id : 6034898056 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following MIPS instructions would you use IDEALLY to divide the value of an integer register by 4 and get the quotient ?

1. div
2. muli
3. sll
4. srl

Options :

60348930199. 1

60348930200. 2

60348930201. 3

60348930202. 4

Question Number : 18 Question Id : 6034898057 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In the MIPS32 assembly language, blt is ____

1. directly supported in hardware
2. a pseudo-instruction translated to a single other hardware instruction
3. is a pseudo-instruction translated to a pair of hardware instructions
4. is supported only if one of the values is zero

Options :

60348930203. 1

60348930204. 2

60348930205. 3

60348930206. 4

Question Number : 19 Question Id : 6034898058 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In MIPS, preserved registers are also called ____ registers.

1. framed
2. callee-saved
3. intermediate
4. temporary

Options :

60348930207. 1

60348930208. 2

60348930209. 3

60348930210. 4

Question Number : 20 Question Id : 6034898059 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In MIPS, preserved registers are saved onto ____.

1. the zeroth memory page
2. dynamic heap memory
3. static global memory
4. stack memory

Options :

60348930211. 1

60348930212. 2

60348930213. 3

60348930214. 4

Question Number : 21 Question Id : 6034898060 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following integer notations has a unique representation for the number 0 ?

1. 0's complement
2. 1's complement
3. 2's complement
4. 32's complement

Options :

60348930215. 1

60348930216. 2

60348930217. 3

60348930218. 4

Question Number : 22 Question Id : 6034898061 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In a MIPS program's memory, the stack data is placed at the bottommost portion (lowest address starting from 0) of memory: ____.

1. only when the program is statically linked
2. only when the program is dynamically linked
3. only when the program has super-user privileges
4. never

Options :

60348930219. 1

60348930220. 2

60348930221. 3

60348930222. 4

Question Number : 23 Question Id : 6034898062 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following is true about the \$at (assembler temporary) register in MIPS32 ?

1. It is unreserved
2. It is reserved, and it is temporarily stored in the swap space
3. It is reserved, and it is temporarily stored in the stack frame
4. It is reserved, but it is not stored in the stack

Options :

60348930223. 1

60348930224. 2

60348930225. 3

60348930226. 4

Question Number : 24 Question Id : 6034898063 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following is true about the \$fp (frame pointer) register in MIPS32 ?

1. It is preserved, and it is temporarily stored in the heap
2. It is preserved, and it is temporarily stored in the swap space
3. It is preserved, and it is temporarily stored in the stack frame
4. It is unreserved

Options :

60348930227. 1

60348930228. 2

60348930229. 3

60348930230. 4

Question Number : 25 Question Id : 6034898064 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In the context of computer performance quantification, SPEC is _____.

1. a particular computer architecture with a parallel computing instruction set
2. a specification language for multi-threaded programs
3. a consortium of computer industries
4. a compiler with all optimization techniques turned off

Options :

60348930231. 1

60348930232. 2

60348930233. 3

60348930234. 4

Question Number : 26 Question Id : 6034898065 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which of the components of the computer performance equation does the choice of algorithm affect ?

1. The number of executed instructions
2. The cycle time of the computer
3. Both the number of executed instructions and the cycle time
4. Neither the number of executed instructions nor the cycle time

Options :

60348930235. 1

60348930236. 2

60348930237. 3

60348930238. 4

Question Number : 27 Question Id : 6034898066 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which of the components of the computer performance equation does the instruction set architecture affect ?

1. Neither the number of instructions nor the CPI
2. Both the number of instructions and the CPI
3. Only the number of instructions
4. Only the CPI

Options :

60348930239. 1

60348930240. 2

60348930241. 3

60348930242. 4

Question Number : 28 Question Id : 6034898067 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following is a valid return statement from an exception handler in a MIPS32 machine?

1. jal \$ra
2. jr \$k1
3. jr \$ra
4. jal \$at

Options :

60348930243. 1

60348930244. 2

60348930245. 3

60348930246. 4

Question Number : 29 Question Id : 6034898068 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Amdahl's law deals with which ONE of the following?

1. The number of possible levels of memory hierarchy
2. The achievable performance improvement in a computer
3. The maximum rate of input/output in a program
4. The maximum number of pipeline stages in a machine

Options :

60348930247. 1

60348930248. 2

60348930249. 3

60348930250. 4

Question Number : 30 Question Id : 6034898069 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Name the entity which converts a HLL (High Level Language) program to assembly language.

1. Operating system
2. Programmer
3. Compiler
4. Editor

Options :

60348930251. 1

60348930252. 2

60348930253. 3

60348930254. 4

Question Number : 31 Question Id : 6034898070 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

A program's CPI (Cycles Per Instruction) will most likely NOT be affected by the use of:

1. integer versus floating point arithmetic
2. signed versus unsigned integers for small positive integer variables
3. optimization techniques employed by the compiler
4. memory versus compute intensive algorithm

Options :

60348930255. 1

60348930256. 2

60348930257. 3

60348930258. 4

Question Number : 32 Question Id : 6034898071 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

The technique of loop unrolling can lead to lesser pipeline stalls. Which entity is responsible for such unrolling?

1. Operating System
2. Dynamic Linker
3. Compiler
4. Terminal Shell

Options :

60348930259. 1

60348930260. 2

60348930261. 3

60348930262. 4

Question Number : 33 Question Id : 6034898072 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Scheduling useful instructions in the branch delay slot is the role of the ____ .

1. Programmer
2. Assembler
3. Compiler
4. Dynamic linker

Options :

60348930263. 1

60348930264. 2

60348930265. 3

60348930266. 4

Question Number : 34 Question Id : 6034898073 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In the MIPS32 5-stage pipeline, what is the ideal CPI (Cycles Per Instruction), in the absence of hazards and stalls?

1. 1/5
2. 1
3. 3
4. 5

Options :

60348930267. 1

60348930268. 2

60348930269. 3

60348930270. 4

Question Number : 35 Question Id : 6034898074 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following techniques is for the purpose of reducing control hazards, and requires the role of the dynamic linker?

1. Branch prediction
2. Early branch completion
3. Branch target buffer
4. None of the above

Options :

60348930271. 1

60348930272. 2

60348930273. 3

60348930274. 4

Question Number : 36 Question Id : 6034898075 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In the MIPS32 5-stage pipeline, an add instruction is followed by a jump instruction. Unconditional branches take 2 cycles to complete. There is NO mechanism other than stalls to deal with control hazards. How many cycles of stall are required and when?

1. 1 cycle, between the add and jump
2. 1 cycle, after the jump
3. 2 cycles, between the add and jump
4. 2 cycles, after the jump

Options :

60348930275. 1

60348930276. 2

60348930277. 3

60348930278. 4

Question Number : 37 Question Id : 6034898076 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following is true about 2-stage branch completion in the MIPS32 5-stage pipeline?

1. This requires the compiler to arrange branch instructions to be within 4 instructions of one another
2. This is possible only for unconditional branches
3. This requires the branch offset to be less than 65536 in absolute value
4. This potentially introduces additional data hazards

Options :

60348930279. 1

60348930280. 2

60348930281. 3

60348930282. 4

Question Number : 38 Question Id : 6034898077 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following is true about 2-stage branch completion in the MIPS32 5-stage pipeline, compared to 3-stage branch completion?

1. Extra data forwarding paths are required
2. Extra delay slots are required
3. Extra instruction formats are required
4. Extra CPU cores are required

Options :

60348930283. 1

60348930284. 2

60348930285. 3

60348930286. 4

Question Number : 39 Question Id : 6034898078 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In the MIPS32 5-stage pipeline, which ONE of the following is true about a STALL introduced due to a data hazard, specifically, lw followed by a dependent sll ?

1. The STALL introduces a nop before the lw in the pipeline
2. The STALL introduces a nop between the lw and the sll in the pipeline
3. The STALL introduces a nop after the sll in the pipeline
4. The STALL introduces two nops: one before and one after the sll in the pipeline

Options :

60348930287. 1

60348930288. 2

60348930289. 3

60348930290. 4

Question Number : 40 Question Id : 6034898079 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In a pipelined processor, what is micro-code ?

1. The first 6 bits of each instruction
2. The code executed by the first 3 stages of the pipeline
3. The code executed by a simpler processor within the main processor, toward implementing pipeline control
4. Any unoptimized machine code

Options :

60348930291. 1

60348930292. 2

60348930293. 3

60348930294. 4

Question Number : 41 Question Id : 6034898080 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Static RAM is generally used in ____.

1. Cache memory
2. Main memory
3. Flash memory
4. Solid state drive

Options :

60348930295. 1

60348930296. 2

60348930297. 3

60348930298. 4

Question Number : 42 Question Id : 6034898081 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In the MIPS32 5-stage pipeline, at the END of which stage can a misaligned data memory access exception be detected?

1. IF
2. ID
3. EX
4. MEM

Options :

60348930299. 1

60348930300. 2

60348930301. 3

60348930302. 4

Question Number : 43 Question Id : 6034898082 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In a computer's cache system, the unit of data transfer into cache during a cache miss is called _____.

1. a page
2. a block
3. a segment
4. a sector

Options :

60348930303. 1

60348930304. 2

60348930305. 3

60348930306. 4

Question Number : 44 Question Id : 6034898083 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which of the following are the kinds of locality in a computer's cache system?

1. L1 and L2
2. L1 and L2 and L3
3. Temporal and spatial
4. Temporal and sectoral

Options :

60348930307. 1

60348930308. 2

60348930309. 3

60348930310. 4

Question Number : 45 Question Id : 6034898084 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

In a cache system, which ONE of the following mechanisms takes advantage of spatial locality?

1. Large tag size
2. Parallel tag comparators
3. Unified I+D cache
4. Multiple words per block

Options :

60348930311. 1

60348930312. 2

60348930313. 3

60348930314. 4

Question Number : 46 Question Id : 6034898085 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

A system has 2MB of main memory and 4KB of cache. It uses a direct mapped scheme and blocks of size 1 word (32 bits). What is the size (number of bits) of the tag field in the memory address? Take $1M = 2^{20}$ and $1K = 2^{10}$.

- 1. 7 bits
- 2. 8 bits
- 3. 9 bits
- 4. 4K bits

Options :

60348930315. 1

60348930316. 2

60348930317. 3

60348930318. 4

Question Number : 47 Question Id : 6034898086 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

If an L1 cache's associativity is changed from 16-way to 8-way, keeping its overall size the same, how is the size of the tag field in a block affected?

- 1. Increases by 2 bits
- 2. Decreases by 8 bits
- 3. Decreases by 16 bits
- 4. Decreases by 1 bit

Options :

60348930319. 1

60348930320. 2

60348930321. 3

60348930322. 4

Question Number : 48 Question Id : 6034898087 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

The number of possible caching schemes based on what happens on a write-hit is ____:

1. two: write-back and write-through
2. two: write-once and write-in-parts
3. exactly one: write-back
4. exactly one: write-once

Options :

60348930323. 1

60348930324. 2

60348930325. 3

60348930326. 4

Question Number : 49 Question Id : 6034898088 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following is TRUE about L1 vs L2 caches?

1. L2 is typically direct mapped, to minimize miss rate
2. L2 is typically larger in size, to minimize miss penalty
3. L2 is typically smaller in size, to minimize miss rate
4. L2 typically has higher associativity, to minimize hit time

Options :

60348930327. 1

60348930328. 2

60348930329. 3

60348930330. 4

Question Number : 50 Question Id : 6034898089 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 1 Wrong Marks : 0

Which ONE of the following techniques can reduce COMPULSORY misses (assuming all other parameters are held constant) ?

1. Increasing associativity
2. Increasing memory width
3. Increasing block size
4. Increasing number of processor cores

Options :

60348930331. 1

60348930332. 2

60348930333. 3

60348930334. 4

Sub-Section Number : 2

Sub-Section Id : 603489293

Question Shuffling Allowed : Yes

Question Number : 51 Question Id : 6034898090 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In the context of L1 cache in a computer, what is the relation between hit ratio and miss ratio?

1. Hit ratio is always $<$ miss ratio
2. Hit ratio is always $>$ miss ratio
3. Hit ratio + miss ratio $<$ 1 always
4. Hit ratio + miss ratio = 1 always

Options :

60348930335. 1

60348930336. 2

60348930337. 3

60348930338. 4

Question Number : 52 Question Id : 6034898091 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

Which ONE of the following results in higher miss penalty in a cache system?

1. Larger block size
2. Using SRAM instead of DRAM
3. Larger memory width
4. Least-recently-used cache replacement scheme

Options :

60348930339. 1

60348930340. 2

60348930341. 3

60348930342. 4

Question Number : 53 Question Id : 6034898092 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In a virtual memory based system, the term "page" refers to: ____

1. the lower portion of main memory
2. a disk sector
3. a disk cylinder
4. the granularity of physical memory allocation

Options :

60348930343. 1

60348930344. 2

60348930345. 3

60348930346. 4

Question Number : 54 Question Id : 6034898093 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In a virtual memory based system, two processes can share memory ____

1. only in the data memory
2. only in the instruction memory
3. only in exception memory
4. in data or instruction memory, in units of a page

Options :

60348930347. 1

60348930348. 2

60348930349. 3

60348930350. 4

Question Number : 55 Question Id : 6034898094 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

Which ONE of the following is an ADVANTAGE of the interleaved memory scheme compared to the original wide-memory scheme?

1. Lower miss penalty
2. Smaller hit time
3. Higher hit rate
4. Lower hardware cost

Options :

60348930351. 1

60348930352. 2

60348930353. 3

60348930354. 4

Question Number : 56 Question Id : 6034898095 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

When someone says they have a 32-bit machine or a 64-bit machine, what does this refer to?

1. The physical memory address length
2. The virtual memory address length
3. The number of floating point registers in the machine
4. The width of the cache-main-memory bus

Options :

60348930355. 1

60348930356. 2

60348930357. 3

60348930358. 4

Question Number : 57 Question Id : 6034898096 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In a computer system, who or which entity maintains the VA-to-PA (Virtual Address to Physical Address) mapping?

1. The programmer, as part of the program logic
2. The compiler, as it compiles the program
3. The cache controller
4. The operating system

Options :

60348930359. 1

60348930360. 2

60348930361. 3

60348930362. 4

Question Number : 58 Question Id : 6034898097 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

Which of the following is the primary purpose of Virtual Memory?

1. Protection of one process's memory from another
2. Faster program execution
3. Cause less page faults
4. Optimal disk utilization

Options :

60348930363. 1

60348930364. 2

60348930365. 3

60348930366. 4

Question Number : 59 Question Id : 6034898098 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

Which ONE of the following metrics is the MOST important to minimize for a TLB ?

1. Hit penalty
2. Hit rate
3. Register utilization
4. Miss penalty

Options :

60348930367. 1

60348930368. 2

60348930369. 3

60348930370. 4

Question Number : 60 Question Id : 6034898099 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

When Virtual Memory is used to provide isolation across processes, ____

1. each process's page table entries are made read-only for other processes
2. each process's page table has mappings to only pages it is allowed to access
3. each process's memory locations are made read-only for other processes
4. when a process is executing, the pages of other processes are moved to secondary memory

Options :

60348930371. 1

60348930372. 2

60348930373. 3

60348930374. 4

Question Number : 61 Question Id : 6034898100 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In an inverted page table scheme, the number of entries (valid or invalid) in the inverted page table would be: Here, V is the number of virtual pages (per process), P is the number of processes in the system, and M is the number of main memory pages.

1. $O(N \times N)$
2. $O(N + P)$
3. $O(M)$
4. $O(M + N)$

Options :

60348930375. 1

60348930376. 2

60348930377. 3

60348930378. 4

Question Number : 62 Question Id : 6034898101 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

Which of the following is/are used as keys in the hashtable mapping, in the inverted page table scheme ?

1. Only Process ID
2. Only the instruction's opcode
3. Instruction's opcode and function code
4. Process ID and Virtual page number

Options :

60348930379. 1

60348930380. 2

60348930381. 3

60348930382. 4

Question Number : 63 Question Id : 6034898102 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In a pipelined processor, TLB access is typically implemented ____ in the common case.

1. by an OS exception handler in a separate processor core
2. in a co-processor
3. in the DMA controller
4. as a pipeline stage, or part of a pipeline stage

Options :

60348930383. 1

60348930384. 2

60348930385. 3

60348930386. 4

Question Number : 64 Question Id : 6034898103 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

The sed tool is used for ____

1. byte-by-byte processing of binary files
2. line-by-line processing of text files
3. filtering records in a database
4. processing object files

Options :

60348930387. 1

60348930388. 2

60348930389. 3

60348930390. 4

Question Number : 65 Question Id : 6034898104 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In a bash script, a '#' represents ____.

1. an array variable
2. the beginning of a comment in a line
3. the beginning of a comment in a line
4. the end of a conditional statement

Options :

60348930391. 1

60348930392. 2

60348930393. 3

60348930394. 4

Question Number : 66 Question Id : 6034898105 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In the context of programming, a “loop invariant” is:

1. A constant which is declared outside the loop
2. A variable whose value does not change inside the loop
3. A condition which must hold at the beginning/end of each loop iteration
4. A #ifndef pre-processor macro defined in a static library

Options :

60348930395. 1

60348930396. 2

60348930397. 3

60348930398. 4

Question Number : 67 Question Id : 6034898106 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In a bash shell, when a program is running in the foreground, to terminate it, which ONE of the following keys/key-sequences must be pressed?

1. Esc
2. Ctrl-Esc
3. Ctrl-Alt-Del
4. Ctrl-C

Options :

60348930399. 1

60348930400. 2

60348930401. 3

60348930402. 4

Question Number : 68 Question Id : 6034898107 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In a bash script, which ONE of the following is used to redirect the STDIN of a process to the STDOUT of another?

1. The hash '#' character
2. The '>' character
3. The '<' character
4. The pipe '|' character

Options :

60348930403. 1

60348930404. 2

60348930405. 3

60348930406. 4

Question Number : 69 Question Id : 6034898108 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In python3, x=3 and y=[4,5]. What does x*y result in?

1. The list [4,5,4,5,4,5]
2. The list [12,15]
3. The list [3,4,5]
4. The list [3,3,3,4,5]

Options :

60348930407. 1

60348930408. 2

60348930409. 3

60348930410. 4

Question Number : 70 Question Id : 6034898109 Question Type : MCQ Option Shuffling : No Is Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

In python, a lambda expression is used to:

1. create a sublist of a given list
2. apply a convolution to elements of a list
3. create a function as a first class object
4. import objects from other libraries

Options :

60348930411. 1

60348930412. 2

60348930413. 3

60348930414. 4

Question Number : 71 Question Id : 6034898110 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

Which ONE of the following is NOT a git command?

1. Merge
2. Branch
3. Glue
4. Commit

Options :

60348930415. 1

60348930416. 2

60348930417. 3

60348930418. 4

Question Number : 72 Question Id : 6034898111 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

The git software tool is used ____

1. For program indentation
2. To identify dead code in a C/C++ program
3. For version management
4. To catch buffer overflow bugs

Options :

60348930419. 1

60348930420. 2

60348930421. 3

60348930422. 4

Question Number : 73 Question Id : 6034898112 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

The yacc tool allows the specification of additional code in which language?

1. C
2. Python
3. Java
4. Javascript

Options :

60348930423. 1

60348930424. 2

60348930425. 3

60348930426. 4

Question Number : 74 Question Id : 6034898113 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

The lex tool can be used to parse any ____

1. C or C++ program
2. Java program
3. context-free grammar
4. regular expression

Options :

60348930427. 1

60348930428. 2

60348930429. 3

60348930430. 4

Question Number : 75 Question Id : 6034898114 Question Type : MCQ Option Shuffling : No Is

Question Mandatory : No

Correct Marks : 2 Wrong Marks : 0

Which ONE of the following is a difference between Object Oriented Programming in C++ versus Java.

1. The feature of exceptions
2. The notion of variables private to a class
3. The notion of interfaces
4. The notion of non-default constructor

Options :

60348930431. 1

60348930432. 2

60348930433. 3

60348930434. 4