PREVIEW QUESTION BANK

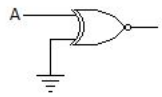
Module Name : nou24-ec03 Digital electronic and System design-ENG
Exam Date : 18-May-2024 Batch : 15:00-18:00

Sr. No.	Client Question ID	Question Body and Alternatives	Marks	Negative Marks
Objective Question				
1	13202001	The $(100110)_2$ is numerically equivalent to 1. $(26)_{16}$ 2. $(36)_{10}$ 3. $(46)_8$ 4. $(212)_4$ The correct answer are 1. 1, 2, and 3 2. 2, 3, and 4 3. 1, 2, and 4 4. 1, 3, and 4 A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
2	13202002	If $(211)_x = (152)_8$, then the value of base x is 1. 6 2. 5 3. 7 4. 9 A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
3	13202003		2.0	0.00

		Which gates in Digital Circuits are required to convert a NOR-based SR latch to an SR flip-flop? 1. Two 2 input AND gates 2. Two 3 input AND gates 3. Two 2 input OR gates 4. Two 3 input OR gates A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
4	13202004	When does a negative level triggered flip-flop in Digital Electronics changes its state? 1. When the clock is negative 2. When the clock is positive 3. When the inputs are all zero 4. When the inputs are all one A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
5	13202005	What is the binary subtraction of 101001 - 010110 =? 1. 010011 2. 100110 3. 011001 4. 010010 A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
6	13202006		2.0	0.00

		The simplified form of a logic function $Y = A(B + C\overline{(AB + AC)})$ is 1. A'B' 2. AB 3. A'B 4. AB' A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
7	13202007	The inputs of a NAND gate are connected together. The resulting circuit is ..... 1. OR 2. NOT 3. AND 4. NAND A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
8	13202008	In 2's complement representation the number 11100101 represents the decimal number ..... 1. +37 2. -31 3. +27 4. -27 A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
9	13202009		2.0	0.00

For the gate in the given figure the output will be .....



1. 0
2. 1
3. A
4. A'

A1 : 1

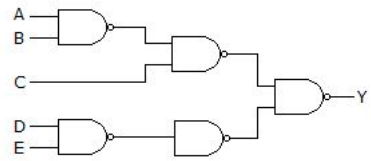
A2 : 2

A3 : 3

A4 : 4

Objective Question

10	13202010	The circuit of the given figure realizes the function	2.0	0.00



1. $Y = (\overline{A} + \overline{B})\,C + \overline{DE}$
2. $Y = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$
3. AB + C +DE
4. AB + C(D + E)

A1 : 1

A2 : 2

A3 : 3

A4 : 4

Objective Question

11	13202011	An AND gate has two inputs A and B and one inhibit input 3, Output is 1 if	2.0	0.00

1. A = 1, B = 1, S = 1
2. A = 1, B = 1, S = 0
3. A = 1, B = 0, S = 1
4. A = 1, B = 0, S = 0

A1 : 1

		A2 : 2 A3 : 3 A4 : 4		
Objective Question				
12	13202012	Which of the following is NOT a type of component available in Tinkercad Circuits? 1. Resistors 2. Transistors 3. Motors 4. Capacitors A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
13	13202013	What is the purpose of the "Start Simulation" button in Tinkercad Circuits? 1. To export the circuit diagram 2. To print a 3D model of the circuit 3. To run a real-time simulation of the circuit behavior 4. To save the circuit to the user's profile A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
14	13202014	Which tool in Tinkercad Circuits allows users to measure voltage and current at different points in the circuit? 1. Multimeter 2. Oscilloscope 3. Function generator 4. Battery A1 : 1 A2 : 2	2.0	0.00

A3 : 3

A4 : 4

Objective Question

15 | 13202015 | 2.0 | 0.00

For the minterm designation Y = ∑ m (1, 3, 5, 7) the complete expression is .....

1. $Y = \overline{A}\,\overline{B}C + A\,\overline{B}\,C$
2. $Y = \overline{A}\,\overline{B}\,C + A\,\overline{B}\,C + ABC + \overline{A}\,BC$
3. $Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,C + \overline{A}BC + A\,\overline{B}C$
4. $Y = \overline{A}\,\overline{B}\,\overline{C} + ABC + \overline{A}\,\overline{B}C + A\,\overline{B}C$

A1 : 1

A2 : 2

A3 : 3

A4 : 4

Objective Question

16 | 13202016 | 2.0 | 0.00

For the K map in the given figure the simplified Boolean expression is .....

AB \ CD	00	01	11	10
00				
01		1		
11		1	1	
10			1	

1. $\overline{A}\,\overline{C} + \overline{A}\,\overline{D} + ABC$
2. $\overline{A}\,C + \overline{A}\,\overline{D} + ABC$
3. $\overline{A}\,C + \overline{A}\,\overline{D} + ACD$
4. $\overline{A}\,\overline{C} + \overline{A}\,\overline{D} + AB\,\overline{C}$

A1 : 1

A2 : 2

A3 : 3

A4 : 4

Objective Question

17 | 13202017 | 2.0 | 0.00

		In a BCD to 7 segment decoder the minimum and maximum number of outputs active at any time is .... 1. 2 and 7 2. 3 and 7 3. 1 and 6 4. 3 and 6 A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
18	13202018	Which of the following logic families typically offers the highest speed performance? 1. TTL 2. ECL 3. CMOS 4. NMOS A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
19	13202019	Which of the following is a characteristic of CMOS logic gates? 1. High input impedance 2. High output impedance 3. Low noise immunity 4. High power consumption A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
20	13202020		2.0	0.00

		Which component of the ALU is responsible for selecting the specific operation to be performed? 1. Multiplexer 2. Comparator 3. Decoder 4. Control Unit A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
21	13202021	What is the primary function of a multiplexer (MUX) in a combinational circuit? 1. Adding numbers 2. Selecting one of many inputs based on control signals 3. Performing logical AND operation 4. Storing data temporarily A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
22	13202022	Which type of ADC is known for its high accuracy but slower conversion speed? 1. Flash ADC 2. Successive approximation ADC 3. Delta-sigma ADC 4. Dual-slope integration ADC A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
23	13202023		2.0	0.00

		Which logic family is known for its low power consumption but suffers from poor noise immunity? 1. TTL 2. CMOS 3. ECL 4. NMOS A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
24	13202024	Which of the following gate is represented by the Boolean expression F =(A'+B')' 1. OR GATE 2. EX-OR GATE 3. AND GATE 4. NOT GATE A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
25	13202025	The dual of A.A' = 0 is 1. A+A' =1 2. A'.A = 1 3. A+A' = 0 4. A'+A = 0 A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
26	13202026		2.0	0.00

		In which logic family does the output voltage directly switch between the power supply rails? 1. TTL 2. CMOS 3. ECL 4. NMOS A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
27	13202027	Which binary code is also known as the weighted code? 1. Excess-3 code 2. Gray code 3. BCD Code 4. ASCII Code A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
28	13202028	In digital logic, a counter is a device which _____ 1. Counts the number of outputs 2. Stores the number of times a particular event or process has occurred 3. Stores the number of times a clock pulse rises and falls 4. Counts the number of inputs A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
29	13202029		2.0	0.00

		What is the maximum possible range of bit-count specifically in n-bit binary counter consisting of 'n' number of flip-flops? 1. 0 to 2^n 2. 0 to $2^n + 1$ 3. 0 to $2^n - 1$ 4. 0 to $2^{n+1/2}$ A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
30	13202030	Ripple counters are also called _____ 1. SSI counters 2. Asynchronous counters 3. Synchronous counters 4. VLSI counters A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
31	13202031	Three decade counter would have _____ 1. 2 BCD counters 2. 3 BCD counters 3. 4 BCD counters 4. 5 BCD counters A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
32	13202032		2.0	0.00

		The full form of SIPO is _____ 1. Serial-in Parallel-out 2. Serial-in Process-out 3. Serial-in Perepheral-out 4. Serial-in Public-out A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
33	13202033	A shift register that will accept a parallel input or a bidirectional serial load and internal shift features is called as? 1. Tristate 2. End around 3. Universal 4. Conversion A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
34	13202034	How can parallel data be taken out of a shift register simultaneously? 1. Use the Q output of the first FF 2. Use the Q output of the last FF 3. Tie all of the Q outputs together 4. Use the Q output of each FF A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
35	13202035		2.0	0.00

		The group of bits 11001 is serially shifted (right-most bit first) into a 5-bit parallel output shift register with an initial state 01110. After three clock pulses, the register contains 1. 01110 2. 00001 3. 00101 4. 00110 A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
36	13202036	A serial in/parallel out, 4-bit shift register initially contains all 1s. The data nibble 0111 is waiting to enter. After four clock pulses, the register contains 1. 0000 2. 1111 3. 0111 4. 1000 A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
37	13202037	Which of the following method is employed for ADC? 1. Ladder network 2. Successive approximation type 3. PWM type 4. None of the mentioned A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
38	13202038		2.0	0.00

		Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature? 1. Cross coupling 2. Gate impedance 3. Synchronous operation 4. Low input voltages A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
39	13202039	The truth table for an S-R flip-flop has how many VALID entries? 1. 1 2. 2 3. 3 4. 4 A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
40	13202040	Which circuit is generated from D flip-flop due to addition of an inverter by causing reduction in the number of inputs? 1. Gated JK-latch 2. Gated D-latch 3. Gated T-latch 4. Gated SR-latch A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
41	13202041		2.0	0.00

		Two J-K flip-flops with their J-K inputs tied HIGH are cascaded to be used as counters. After four input clock pulses, the binary count is 1. 00 2. 11 3. 01 4. 10 A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
42	13202042	Which statement describes the BEST operation of a negative-edge-triggered D flip-flop? 1. The Q output is ALWAYS identical to the CLK input if the D input is HIGH 2. The logic level at the D input is transferred to Q on NGT of CLK 3. The Q output is ALWAYS identical to the D input when CLK = PGT 4. The Q output is ALWAYS identical to the D input A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
43	13202043	The only difference between a combinational circuit and a flip-flop is that 1. The flip-flop requires previous state 2. The flip-flop requires next state 3. The flip-flop requires a clock pulse 4. The flip-flop depends on the past as well as present states A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
44	13202044		2.0	0.00

In JK flip flop same input, i.e. at a particular time or during a clock pulse, the output will oscillate back and forth between 0 and 1. At the end of the clock pulse the value of output Q is uncertain. The situation is referred to as?

1. Conversion condition
2. Race around condition
3. Lock out state
4. Forbidden State

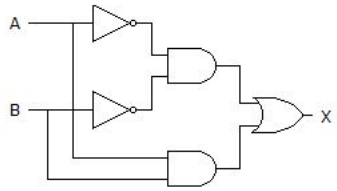
A1 : 1

A2 : 2

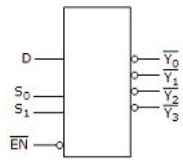
A3 : 3

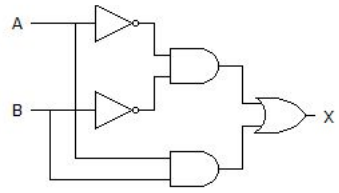
A4 : 4

Objective Question

45	13202045	Which of the following logic expressions represents the logic diagram shown?  1. X=AB'+A'B 2. X=(AB)'+AB 3. X=(AB)'+A'B' 4. X=A'B'+AB A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00

Objective Question

46	13202046	The device shown here is most likely a  1. Comparator 2. Multiplexer 3. Inverter 4. Demultiplexer	2.0	0.00

		A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
47	13202047	What type of logic circuit is represented by the figure shown below  1. XOR 2. XNOR 3. AND 4. NAND A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
48	13202048	How many NOT gates are required for the construction of a 4-to-1 multiplexer? 1. 3 2. 4 3. 2 4. 5 A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00
Objective Question				
49	13202049		2.0	0.00

		In 1-to-4 demultiplexer, how many select lines are required 1. 2 2. 3 3. 4 4. 5 A1 : 1 A2 : 2 A3 : 3 A4 : 4		
Objective Question				
50	13202050	S-R type flip-flop can be converted into D type flip-flop if S is connected to R through 1. OR Gate 2. AND Gate 3. Inverter 4. Full Adder A1 : 1 A2 : 2 A3 : 3 A4 : 4	2.0	0.00